REMARKS

Entry of this Amendment in accordance with the provisions of 37 CFR §1.114 is respectfully requested, noting that this Amendment is being filed as a Submission with a Request for Continued Examination (RCE) on even date herewith.

This Amendment is in response to the Final Office Action dated November 6, 2006. By the present Amendment, each of the independent claims 1-5 have been amended to further clarify the invention, as will be discussed below.

Reconsideration and removal of the rejection of claims 1-5 over USP 5,732,236 to Nguyen is respectfully requested. By the present Amendment, each of the independent claims 1-5 has been amended to define the feature of the invention that:

> "wherein said plurality of banks are formed on a single chip, and wherein said random access memory is adapted to share control signals received by said random access memory, from said memory control means, among said plurality of banks."

This Amendment corresponds, for example, to the discussion on page 14, lines 11-16 of the Specification which states:

> "The system configuration can be implemented with a single LSI by integrating the memory controller 1, the RU3, the DU4, the VU5 and the IOU6. The CPU2 may also be added to and integrated with these component parts to implement a single LSI. Further, the memory 7 may be added to realize the single LSI."

In conjunction with this, page 13, line 27 et seq. defines the memory being divided into a plurality of banks, each bank being further divided into a plurality of pages. Since the memory 7 is formed on a single chip, the plurality of banks forming the memory 7 must, of necessity, also be formed on a single chip. In addition, as shown in Fig. 1, the control signals (e.g., RAS, CAS, WE, etc.) from the memory control unit 11 are provided to the memory 7, and, as such, will be shared among the plurality of banks making up the memory 7. This arrangement is completely opposite to the

arrangement taught by Nguyen since Nguyen fails to teach forming the plurality of banks on a single chip, and also discloses providing independent control signals (e.g., RAS, CAS, WE, etc.) to each of the individual banks. The arrangement utilizing independent control signals, rather than shared control signals, is clearly seen in the left side of Fig. 1 in the system memory 11 of Nguyen. As an example, the first bank 30 receives control signals RAS1, CAS 1 and WEZ1 whereas the second bank 31 receives independent control signals RAS2, CAS2 and WEZ2. Similarly, in the example of Fig. 3b of Nguyen, the controller outputs a W/R command to bank 3 while simultaneously outputting a precharge command to bank 1 by virtue of these independent signals. As such, Nguyen fails to teach or suggest the claimed feature of providing the plural banks on a single chip and providing an arrangement in which the control signals are shared among the plural banks. Therefore, the claim limitations of claims 1-5 requiring executing before a next request for access to a page to be accessed subsequently by the processor, precharge of the page to be accessed subsequently must be taken within the overall context of the plurality of banks being formed on the same chip and sharing the control signals from the memory controller. Nguyen simply fails to either teach this claim structure or the resulting operation and advantages.

In addition to the above distinction, it is further noted that each of the independent claims 1-5 has been amended to define that the random access memory is a single memory, as disclosed on page 13, line 8. This is distinctly different than the arrangement in Nguyen in which the plural banks are clearly formed of plural DRAMs. For example, column 2, lines 61 and 62 of Nguyen state:

> "A system memory 11 implemented with a plurality of dynamic random access memory (DRAM) units."

Similarly, in column 3, line 8 et seq., Nguyen states:

> "System memory 11 comprises four memory banks illustrated in Fig. 1 as first bank 30, second bank 32, third bank 34 and fourth bank 36. Each of the first bank 30, second bank 32, third bank 34 and fourth bank 36 may comprise one or more DRAM units."

Therefore, in Nguyen each bank is a separate DRAM, whereas in the present invention, as defined by the amended claims, a single DRAM is divided into a plurality of banks, all of which are formed on a single chip and all of which share control signals from the memory controller. As such, the amended claims clearly emphasize structural distinctions of the present invention over Nguyen, and, accordingly, reconsideration and allowance of the amended independent claims 1-5 is earnestly solicited.

If the Examiner determines that there are any matters which can be resolved by way of either a personal or telephone interview, the Examiner is invited to contact Applicants' undersigned attorney at the number indicated below.

Applicants request any shortage or excess in fees in connection with the filing of this paper, including extension of time fees, and for which no other form of payment is offered, be charged or credited to Deposit Account No. 01-2135 (Case: 500.40687CX1).

Respectfully submitted,
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